

(1) TITLE

ESD Protection for Integrated Circuits

(2) CROSS-REFERENCE TO RELATED APPLICATIONS

Not applicable.

(3) STATEMENT REGARDING FEDERALLY SPONSORED RESEARCH OR
DEVELOPMENT

Not applicable.

(4) REFERENCE TO AN APPENDIX

Not applicable.

(5) BACKGROUND

TECHNICAL FIELD

[0001] This disclosure relates generally to integrated circuits and more particularly to electrostatic discharge protection for integrated circuits.

DESCRIPTION OF RELATED ART

[0002] Electrostatic discharge ("ESD") is a well known concern with respect to the design and implementation of integrated circuits ("IC" or "chip"). ESD events occur when very large electrical spikes, potentially reaching thousands of volts, occur on an input-output ("I/O") terminal, "pad," of the chip which is designed for an operating voltage of just a few volts. Such ESD spikes can damage or destroy the IC components, rendering it defective or useless. Therefore, ICs are frequently designed to provide some sort of protection against ESD events.

[0003] The ESD problem is particularly egregious in metal-oxide-semiconductor ("MOS") and complementary-metal-oxide-semiconductor ("CMOS") integrated

1 circuits. FIGURE 1C (Prior Art) is an electrical schematic block diagram
2 illustrating a typical input-output ("I/O") pad and VCC pad scheme. While
3 exemplary structures, elements, and devices are discussed in detail hereinafter, it
4 will be recognized by those skilled in the art that specific implementations will vary
5 depending on the specific design criteria, e.g., size, operating voltage, "VCC,"
6 and current requirements, and the like, and fabrication processes for any NMOS,
7 PMOS, CMOS, and BiCMOS type integrated circuit implementations; no limitation
8 on the scope of the invention is intended by the inventor by use of the following
9 examples, nor should any be implied therefrom.

10 [0004] It is known in the art to use surface diodes, Zener diodes and Schottky
11 diodes to protect against IC damage due to ESD events; see e.g. U.S. Patent No.
12 5,412,527 (Husher), assigned to the common assignee hereof.

13 [0005] FIGURES 1A (Prior Art) and 1B (Prior Art) illustrate conventional MOSFET
14 structures 100N, 100P, respectively; depicting a pair of a larger MOSFET array
15 commonly found in ICs. In conventional input-output ("I/O") cells of a CMOS chip,
16 it is known to use a pull-up, field effect transistor ("FET") - see e.g., a P-type
17 dopant source/ drain, P-channel, MOSFET (hereinafter "P-MOSFET" for short)
18 100P - and a pull-down transistor - see e.g., a N-type dopant source/drain, N-
19 channel, MOSFET (hereinafter "N-MOSFET" for short) 100N - in push-pull circuit
20 configurations either to drive a signal off-chip or to receive and condition external
21 inputs to the chip circuitry. It is known to combine the push-pull transistor pair
22 with the circuitry shown by Husher, supra, to protect the internal IC circuitry from
23 ESD events which can be for example as high as 200 Volts in a machine model

1 or 2000 Volts in a human body model.

2 [0006] Referring again to FIGURE 1A, with a N-MOSFET structure 100N - with
3 "D" designating drain region and contact, "G" designating gate region and
4 contact, and "S/B" designating source/body region and contact - used in I/O cells,
5 ESD event device breakdown occurs along the N+ doped common drain region
6 101 and gate polysilicon 103, 103' interfaces at the epitaxial layer, "P-epi/P-well"
7 105, surface 105'. Similarly referring to FIGURE 1B, with a P-MOSFET structure
8 100P, ESD event device breakdown occurs along the P+ doped drain region 107
9 to gate polysilicon region 103, 103' interfaces 109, 109'.

10 [0007] However, newer electronic appliance applications, such as allowing
11 computer peripheral plug-in during computer operation - also known as "hot plug-
12 ins" (e.g., plugging a printer into a laptop computer without first turning off the
13 appliances), "hot swaps" (e.g., exchanging a floppy disk drive for a CD drive),
14 USB port On-The-Go uses, power over an Ethernet connection, and the like, all
15 have a potential for even much higher ESD events, e.g., up to 15,000 Volts,
16 human body model. Thus, these newer appliances have a need for IC devices
17 having concomitant ESD ratings.

18 (6) BRIEF SUMMARY

19 [0008] The basic aspects of the invention generally provide circuitry and IC
20 device structures for improving ESD protection for integrated circuits.

21 [0009] In one aspect, an exemplary embodiment of the present invention
22 provides semiconductor MOSFET structure having improved ESD tolerance, the
23 structure including: a semiconductor substrate having an active device surface; in

1 said surface, a MOSFET source region and a MOSFET drain region separated by
2 a channel region; a P-type dopant region subjacent said drain region and having
3 a dopant concentration and predetermined dimensions such inherent parasitic
4 transistor gain of said MOSFET structure is increased.

5 [0010] In another aspect, an exemplary embodiment of the present invention
6 provides an integrated circuit ESD protection device for an IC I/O pad, the device
7 including: a N-MOSFET; a P-MOSFET, wherein said N-MOSFET and P-MOSFET
8 are connected in a push-pull configuration with drain regions thereof connected to
9 said I/O pad; and both said N-MOSFET and said P-MOSFET including a P-type
10 dopant region substantially subjacent respective the drain regions of each such
11 that P-MOSFET parasitic PNP transistor gain and N-MOSFET parasitic NPN
12 transistor gain is increased thereby.

13 [0011] In another aspect, an exemplary embodiment of the present invention
14 provides an ESD protection circuit for an IC having at least one I/O pad and at
15 least one VCC pad having a electrically grounded ESD protection device
16 connected thereto, the circuit including: a N-GCMOSFET having a first drain
17 region connected to said I/O pad, a first gate region connected to electrical
18 ground, and a first source region connected to electrical ground; and a P-
19 GCMOSFET having a second drain region connected to said I/O pad, a second
20 gate region connected to said VCC pad, and a second source region connected
21 to said VCC pad, wherein said first drain region has a P-type dopant region
22 substantially subjacent thereto for enhancing parasitic NPN transistor gain
23 thereof, and said second drain region has a P-type dopant region substantially

1 subjacent thereto for enhancing parasitic PNP transistor gain thereof.

2 [0012] In another aspect, an exemplary embodiment of the present invention
3 provides a N-channel MOSFET structure for ESD device, the structure including:
4 a P-doped substrate having an epitaxial layer for forming active device elements
5 therein; and within said epitaxial layer, a N+ doped source region; a N+ drain
6 region; a P-doped channel region between the source region and the drain
7 region; a gate superjacent the channel; an N-doped well region beneath said
8 drain region having a width dimension less than a width dimension of said drain
9 region; and a P-doped deep region, beneath said drain region and adjacent said
10 well region, having a dopant concentration greater than said P-doped channel
11 region, wherein said P-doped deep region increases gain of a parasitic lateral
12 NPN transistor formed by said source region, said channel region and said drain
13 region and lowers triggering voltage of said MOSFET.

14 [0013] In another aspect, an exemplary embodiment of the present invention
15 provides a P-channel MOSFET structure for an ESD protection circuit, the
16 structure including: a P-doped substrate having an epitaxial layer; a N-doped well
17 in said epitaxial layer for forming active device elements therein; and within said
18 N-doped well, a P+ doped source region; a P+ drain region; a N-doped channel
19 region between the source region and the drain region; a gate superjacent the
20 channel; and a P-doped deep region, beneath said drain region and adjacent
21 said well region, wherein said P-doped deep region increases gain of a parasitic
22 PNP transistor formed by said drain region, N-doped well region and said
23 epitaxial layer and lowers triggering voltage of said MOSFET.

1 [0014] In another aspect, an exemplary embodiment of the present invention
2 provides a MOSFET structure for an ESD protection circuit, the structure
3 including: a substrate having an epitaxial layer forming an active device surface;
4 at least two MOSFETs proximate said surface, each MOSFET having a first
5 dopant type drain region wherein said drain regions are adjacent and separated
6 by a region of said surface and forming diode poles thereby; and a second
7 dopant type deep region at said region of the surface, wherein said deep region
8 has a depth from said surface into said epitaxial layer greater than a depth of
9 each of said drain regions such that an ESD spike causes a diode breakdown to
10 the epitaxial layer before affecting the MOSFETs.

11 [0015] In another aspect, an exemplary embodiment of the present invention
12 provides a MOSFET structure for an ESD protection circuit employing an SCR,
13 the structure located in an epitaxial layer of a first dopant type of a substrate, said
14 epitaxial layer having an active device surface, the structure including: a first
15 MOSFET of a second dopant type located proximate said surface and having a
16 first drain region of the second dopant type; a second MOSFET of the second
17 dopant type and located proximate said surface and having a second drain region
18 of the second dopant type proximate said first drain region; a drain contact
19 electrically connecting said first drain region and said second drain region; a
20 surface contact region abutting said drain contact and separating said first drain
21 region said second drain region, said surface region having said first dopant type;
22 subjacent the surface contact region and within said epitaxial layer, a well of said
23 second dopant type, wherein said well is subjacent both said first drain region

1 and said second drain region; and within said well, a deep region of P-type ion
2 dopant, wherein said deep region is subjacent both said first drain region, said
3 second drain region, and said surface contact region, wherein said deep region
4 dimensions and concentration of the P-type ion are predetermined for achieving a
5 desired SCR punch-through voltage via tuning breakdown fields and improving
6 structure inherent bipolar transistor gain accordingly.

7 [0016] In another aspect, an exemplary embodiment of the present invention
8 provides a BiCMOS technology N-MOSFET structure for ESD protection circuits,
9 the structure including: a P ion doped substrate; an N ion doped epitaxial layer
10 superjacent said substrate, said epitaxial layer having an upper surface distal
11 from said substrate; a buried isolation layer; a P ion doped well subjacent in said
12 upper surface; a N+ ion doped source region subjacent said surface; a N+ ion
13 doped drain region subjacent said surface; a region of said well forming a P ion
14 channel region at said surface between said source region and said drain region;
15 a gate structure superposing said channel region; and subjacent said drain region
16 and within said well, a P ion doped deep region, said deep region having an ion
17 concentration greater than ion concentration of said well, such that lateral bipolar
18 parasitic NPN transistor of said structure is provided with increased gain by the
19 deep region.

20 [0017] In another aspect, an exemplary embodiment of the present invention
21 provides a BiCMOS technology P-MOSFET structure for ESD protection circuits,
22 the structure including: a P ion doped substrate; an N ion doped epitaxial layer
23 superjacent said substrate, said epitaxial layer having an upper surface distal

1 from said substrate; a buried isolation layer; a N ion doped well subjacent in said
2 upper surface; a P+ ion doped source region subjacent said surface; a P+ ion
3 doped drain region subjacent said surface; a region of said well forming a N ion
4 channel region at said surface between said source region and said drain region;
5 a gate structure superposing said channel region; and subjacent said drain region
6 and within said well, a P ion doped deep region, said deep region having an ion
7 concentration substantially equal to or greater than ion concentration of said drain
8 region, such that vertical bipolar parasitic PNP transistor of said structure is
9 provided with increased gain by the deep region.

10 [0018] In another aspect, an exemplary embodiment of the present invention
11 provides a BiCMOS technology structure for a push-pull I/O ESD protection circuit
12 employing an SCR, the structure located in an epitaxial layer of a first dopant type
13 of a substrate of a second dopant type, said epitaxial layer having an active
14 device surface, the structure including: a first dopant type buried layer
15 segregating said epitaxial layer and said substrate; a second dopant type first
16 well within said epitaxial layer and subjacent said surface; a second dopant type
17 second well within said epitaxial layer and subjacent said surface; a first dopant
18 type third well within said epitaxial layer and subjacent said surface, such that
19 third well is adjacently between said first well and said second well; a first
20 MOSFET of the first dopant type located within said first well proximate said
21 surface and having a first drain region of the first dopant type and having a
22 predetermined drain width for superjacently spanning a first area of said surface
23 encompassing surface regions of both said first well and said third well; a second

1 MOSFET of the first dopant type and located within said second well proximate
2 said surface and having a second drain region of the first dopant type and having
3 a predetermined drain width for superjacently spanning a second area of said
4 surface encompassing surface regions of both said third well and said second
5 well; a drain contact electrically connecting said first drain region and said second
6 drain region; a surface contact region abutting said drain contact and separating
7 said first drain region said second drain region, said surface region having said
8 second dopant type; within said third well, a deep region of P-type ion dopant,
9 wherein said deep region is subjacent both said first drain region, said second
10 drain region, and said surface contact region, wherein said deep region
11 dimensions and concentration of the P-type ion are predetermined for achieving a
12 desired SCR punch-through voltage via tuning breakdown fields and improving
13 structure inherent bipolar transistor gain accordingly.

14 [0019] In another aspect, an exemplary embodiment of the present invention
15 provides an extended drain N-channel MOSFET structure including: a P-type
16 substrate; in said substrate at least one MOSFET structure having extended and
17 enhanced drain region devices for providing reduced on-resistance at a surface
18 region of said substrate, said MOSFET structure including an N+ doped drain
19 region in an N-type well region; and a P-deep region subjacent the N-well
20 containing the drain region, said P-deep region having geometry and a dopant
21 concentration such that said P-deep region increases gain of a parasitic lateral
22 NPN transistor and lowers triggering voltage of said MOSFET.

23 [0020] The foregoing summary is not intended to be inclusive of all aspects,

1 objects, advantages and features of the present invention nor should any
2 limitation on the scope of the invention be implied therefrom. This Brief Summary
3 is provided in accordance with the mandate of 37 C.F.R. 1.73 and M.P.E.P.
4 608.01(d) merely to apprise the public, and more especially those interested in
5 the particular art to which the invention relates, of the nature of the invention in
6 order to be of assistance in aiding ready understanding of the patent in future
7 searches.

8 (7) BRIEF DESCRIPTION OF THE DRAWINGS

9 [0021] FIGURE 1A (Prior Art) is a cross-sectional, elevation view, schematic of a
10 conventional N-channel MOSFET.

11 [0022] FIGURE 1B (Prior Art) is a cross-sectional, elevation view, schematic of a
12 conventional P-channel MOSFET.

13 [0023] FIGURE 1C (Prior Art) is an electrical schematic block diagram illustrating
14 a typical input-output ("I/O") pad and VCC pad scheme.

15 [0024] FIGURE 2A is a cross-sectional, elevation view, schematic of a N-channel
16 MOSFET structure in accordance with an exemplary embodiment of the present
17 invention.

18 [0025] FIGURE 2B is a cross-sectional, elevation view, schematic of a P-channel
19 MOSFET structure in accordance with an exemplary embodiment of the present
20 invention.

21 [0026] FIGURE 3 is a push-pull I/O circuit diagram in accordance with another
22 exemplary embodiment of the present invention employing MOSFETs using the
23 structure 200N of FIGURE 2A and structure 200P FIGURE 2B.

1 [0027] FIGURE 4 is a cross-sectional, elevation view, schematic of a N-channel
2 MOSFET structure including a surface diode/Zener diode in another exemplary
3 embodiment in accordance with the present invention.

4 [0028] FIGURE 5 is a N-channel MOSFET structure with integrated silicon
5 controlled rectifier ("SCR") exemplary embodiment in accordance with the present
6 invention in a cross-sectional, elevation view.

7 [0029] FIGURE 6A is a cross-sectional, elevation view, schematic of another N-
8 channel MOSFET structure used typically in BiCMOS technology in another
9 exemplary embodiment of the present invention.

10 [0030] FIGURE 6B is a cross-sectional, elevation view, schematic of another P-
11 channel MOSFET structure used typically in BiCMOS technology in another
12 exemplary embodiment of the present invention.

13 [0031] FIGURE 7 is a cross-sectional, elevation view, schematic of a BiCMOS
14 structure with integrated silicon controlled rectifier in another exemplary
15 embodiment in accordance with the present invention.

16 [0032] FIGURE 8 is a cross-sectional, elevation view, schematic of an extended
17 drain N-channel MOSFET structure in another exemplary embodiment in
18 accordance with the present invention.

19 [0033] FIGURE 9 is a cross-sectional, elevation view, schematic of a single N-
20 MOSFET structure in another exemplary embodiment in accordance with the
21 present invention.

22 [0034] Like reference designations represent like features throughout the
23 drawings. The drawings in this specification should be understood as not being

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1 drawn to scale unless specifically annotated as such.

(8) DETAILED DESCRIPTION

[0035] In general, the present invention uses at least one P-type, implantation region, or layer, referred to hereinafter as "P-deep," in both NMOS and PMOS devices to enhance ESD protection performance. The present invention is particularly suited to enhancing ESD protection performance for I/O cells and power supply clamps used in CMOS and BiCMOS IC technologies.

[0036] A cross-sectional, elevation view schematic of a pair of adjacent N-MOSFET 200N structures in accordance with an exemplary embodiment of the present invention is shown in **FIGURE 2A**. It should be recognized that this drawing represents a small region of input/output structures of a complete IC, viz., part of an array of I/O cells, or the like as would be known in the art. It should be recognized that many publications describe the details of common techniques used in the fabrication process of integrated circuit components. See, e.g., Wolf, S., *Silicon Processing for the VLSI Era*, copyright 1990, Lattice Press; Sze, S.M., *VLSI Technology*, copyright 1988, McGraw-Hill; Ghandhi, S.K., *VLSI Fabrication Principles*, copyright 1983, John Wiley & Sons; or *Semiconductor & Integrated Circuit Fabrication Techniques*, Reston Publishing Co., Inc., copyright 1979 by the Fairchild Corporation. Those known manner techniques are generally employed in the fabrication of the structure of the present invention except in the steps required to accomplish the goals of the present invention; as such, an in depth description of known manner steps is unnecessary to an understanding of the present invention. Moreover, the individual steps of such a process can be performed using commercially available integrated circuit fabrication machines.

1 See, e.g., Chapman, B., *Glow Discharge Processes/Sputtering and Plasma*
2 *Etching*, copyright 1980, John Wiley & Sons. As specifically helpful to an
3 understanding of the present invention, approximate technical data are set forth
4 based upon current technology. Future developments in this art may call for
5 appropriate adjustments as would be obvious to one skilled in the art. It will be
6 intuitively obvious to a person skilled in the art that the invention taught herein will
7 have wide applicability to integrated circuit fabrication processes; this description
8 relies on an exemplary implementation of industrial applicability and no limitation
9 on the scope of the invention is intended nor should any be implied therefrom.

10 [0037] On a P-type doped substrate 201, having a surface 203, a P-type doped
11 epitaxial layer 205 ("P-epi") is formed wherein IC active devices will be fabricated
12 in a known manner. Using conventional, grown field oxide ("FOX") regions 207,
13 207' for masking, a P-type doped "P-well" 209 is formed. Relatively high
14 concentration, "designated N+," N-type doped source, "S," regions 211, 211' and
15 a common drain, "D," region 213 are formed within the P-well 209. Also
16 conventionally, respective transistor gates, "G," 217, 217' are formed in
17 respective gate polysilicon 219, 219' superjacent epitaxial surface 205' and the N-
18 MOSFET source-drain N-channel regions in the epitaxial P-well 209, respectively.
19 In a known manner commonly referred to as "Metal 1" process steps, conductor
20 traces 221, 221', 215 and electrical contacts are formed for respective
21 source/body, "S/B," and drain regions of the MOSFET structure 200. P+ doped
22 body regions 220, 220' complete the traditional elements of the dual N-MOSFET
23 cell structure 200N.

1 [0038] "N-well" 223 is formed in the P-well 209 subjacent the drain contact 215,
2 bridging the drain to the P-epi layer 205. This deep N-well 223 facilitates
3 reduction of current density in the N+ regions and reduction of heating of the
4 contacts to avoid metal spiking into the silicon, which would result in junction
5 leakage or short. Generally, the cross-sectional width of the deep N-well 223 is
6 in the range of approximately two to three times the width of the drain contact 215
7 surface region. The N-type ion concentration is less than that of the source/drain
8 concentration by a factor in the approximate range of $1E3$ to $1E4$.

9 [0039] A deep implant of P-type dopant is made in order to form "P-deep" regions
10 225, 225'. While implant concentration will be process specific, generally it may
11 be considered that the surface concentration of the dopant ions in the P-deep
12 regions 225, 225' should be approximately an order of magnitude greater than
13 that of the dopant ions at the P-well 209 surface concentration. Similarly, the
14 respective junction depth of the P-well 209 and P-deep regions 225, 225' will be
15 process dependent. In general, as will be discussed in more detail hereinafter,
16 particularly with respect to FIGURE 3, the design goal is to improve parasitic
17 transistor performance to enhance ESD protection. Note, particularly in the case
18 of a push-pull I/O circuit embodiment, that this is directly contrary to conventional
19 wisdom, which seeks to suppress parasitic transistor gain.

20 [0040] The P-deep regions 225, 225' are formed subjacently to the drain region
21 213 and adjacently to the sub-drain N-well region 223. That is, the deep P-
22 dopant implant is done proximate to both the N+ drain region and the N-well
23 region-to-drain interface. This structure produces high electric field areas across

1 the N+ drain 213 to P-deep interfaces 227, 227'. Thus, heat from current flow
2 under junction breakdown conditions during an ESD event is positioned distally to
3 the drain contact to avoid contact metal spiking. There is a higher drain-to-
4 substrate inherent capacitance and enhanced parasitic NPN transistor gain in
5 breakdown of the structure of FIGURE 2A compared to FIGURE 1A, providing a
6 lower trigger voltage for the N-MOSFETs, and enhancing ESD protection. This
7 will be explained further with respect to FIGURE 3.

8 [0041] It is recognized and noted that while higher drain-to-substrate capacitance
9 is good for ESD protection, it affects rise-time and fall-time on the input-output
10 pads. This should be taken into consideration for any specific design
11 implementation. Nonetheless, the present invention has been found to greatly
12 scalable for appliances where high ESD immunity is necessary. In most of the
13 embodiments described herein, because the P-deep region is incorporated within
14 the basic 225, 225' traditional MOSFET structure, there is no requirement for
15 using of valuable epitaxial surface area.

16 [0042] Turning to FIGURE 2B, a structure 200P is illustrated for P-MOSFETs in
17 accordance with another embodiment of the present invention. As would be
18 known in the art, for a PMOS device the implant dopants for the traditional FET
19 elements, the epi-well 209_N, the source regions 211_P, 211_P' and drain region 213_P,
20 are the opposite of the NMOS devices of FIGURE 2A. Another difference is that
21 the drain region 213_P is not expanded in width as was the case in the NMOS
22 devices of FIGURE 2A. Therefore, in accordance with this exemplary
23 embodiment, a single P-deep implant region 225_P can be formed subjacently to

1 the P-type drain region 213_P directly in the N-well 209_P. For P-MOSFETs, the P-
2 deep region provides an improved parasitic PNP transistor gain that enhances
3 ESD protection.

4 [0043] Now turning to **FIGURE 3**, an equivalent circuit for a pull-up P-MOSFET
5 and pull-down N-MOSFET I/O circuit 300 employing the present invention is
6 depicted. The FIGURE is illustrative of one I/O pad 301 of a chip having many
7 such input-outputs for the associated chip circuitry (not shown other than "To ckt."
8 node 303). The chip operating voltage, VCC, is provided via a conventional VCC
9 pad 305. The VCC pad 305 is shown having an ESD protection circuit
10 comprising a conventional N-channel MOSFET 307 - viz., such as shown in
11 **FIGURE 1A** - in a source-gate-coupled, "GC," grounded-gate, "GG,"
12 configuration, with its gate grounded via resistor R1; see also, **FIGURE 2A**, 200N.
13 A drain to P-well to source, lateral, bipolar, parasitic NPN transistor of the
14 MOSFET 307 is shown in phantom-line.

15 [0044] A P-deep, P-MOSFET 200P, in accordance with the structural
16 embodiment described above with respect to **FIGURE 2B**, connects the VCC pad
17 305 and the I/O pad 301. The P-MOSFET 200P is gate-coupled, with the gate,
18 G, electrically tied to the VCC pad, via node 309, and to the source, S. The drain,
19 D, is electrically connected, via node 311, to the I/O pad 301. This P-
20 GCMOSFET 200P has a drain-to-well-to-epi/substrate bipolar parasitic PNP
21 transistor 313 shown in phantom line. Effectively, the parasitic PNP transistor
22 313 has a grounded collector, C, since the P-type substrate is electrical ground, a
23 base, B, derived from the N-well body of the P-GCMOSFET 200P electrically

1 connected to the source, S, and emitter, E, derived from the P-GCMOSFET 200P
2 drain, D. Addition of the P-deep implant 225_p, FIGURE 2B, subjacent the drain
3 region 213_p of the P-GCMOSFET 200P effectively increases the gain of the
4 parasitic PNP transistor 313.

5 [0045] Also electrically tied via node 311 to the I/O pad 309 is the drain, D, of a
6 P-deep, N-GCMOSFET 200N as shown in FIGURE 2A. The gate, G, of transistor
7 200N is connected to ground via a resistor R2. The source, S, of transistor 200N
8 is connected directly to ground and effectively to the gate, G, via the resistor R2.
9 The N-GC-MOSFET 200N has a lateral, bipolar, parasitic NPN transistor 315
10 deriving its emitter, E, from the N-MOSFET 200N source, S, its collector from the
11 drain, D, and its base, B, at ground from the P-well.

12 [0046] This push-pull arrangement of FIGURE 3 connected to the I/O pad 301 via
13 node 311 thus employs the structures shown in FIGURES 2A and 2B. As in
14 FIGURE 2A, the parasitic NPN transistor 315, FIGURE 3, is formed by N-type
15 drain 213, grounded N-type source 211, and P-well 209. In FIGURE 2B, the
16 parasitic PNP transistor 313 is formed by P-deep region 225_p, N-well 209_p, P-
17 epi205/P-substrate 201.

18 [0047] For P-MOSFET implementations, by use of P-deep implant, the effective
19 base width of parasitic transistors is reduced since the substrate-to-drain spacing
20 is reduced. For N-MOSFET implementations, the P-deep region enhances
21 capacitance and parasitic NPN gain during breakdown.

22 [0048] In operation, when the I/O pad 301 experiences an ESD, the P-type
23 drain, D, acting as the emitter, E, to source, S, acting as base, B, forms a diode

1 of the P-GCMOSFET 200P that gets forward biased such that part of the ESD
2 event current is shunted to ground via the P-epi 205 and substrate 201 layers.
3 Note also, that part of the current from the ESD event on the I/O pad 301 will flow
4 through the P-MOSFET channel to pad 305, through the parasitic PNP transistor
5 313 of the GC-MOSFET 200P to ground via the ESD protection circuit on the
6 VCC pad 305, as its parasitic NPN transistor is turned ON, and through N-GC-
7 MOSFET 200N; the parasitic NPN transistor 315 of GC-MOSFET 200N turns on
8 during an ESD event. Effectively, the P-deep region 225, 225' increases the
9 inherent capacitance to ground of the N-GCMOSFET 200N. Again, ESD current
10 is shunted from node 311 to ground.

11 [0049] Thus, three paths are conducting ESD current to ground and away from
12 node 303 and the internal circuitry of the integrated circuit chip.

13 [0050] Another embodiment is depicted by the structure 400 of **FIGURE 4**
14 employing a diode such as taught by Husher, supra. It has been found that
15 altering such known structures enhances ESD protection. A surface diode
16 element is formed by surface metal 401 and the neighboring contacted N+ doped
17 regions 403, 405 forming the cathode and anode in the P-well 209 of the P-epi
18 layer 205. Note that the N+ doped regions 403, 405 also form the drains of a pair
19 of traditional N-channel MOSFETs 407, 409. From FIGURE 3 it can be seen that
20 a ESD input spike to the I/O pad 301 is connected to the drains of the push-pull
21 MOSFETs 200P, 200N at their respective drain, D, contacts. A P-deep region
22 425 is implanted between the adjacent N+ doped regions 403, 405, preferably
23 extending into the P-well 209 to a depth at least equal to or preferably greater

1 than the depth of the N+ doped regions. The dimensions of the P-deep region
2 425 can be designed to specific implementations for tailoring the breakdown
3 voltage. An ESD spike will thus allow a diode breakdown through the P-well 209
4 to the P-epi/P-substrate 205, 201 before affecting the MOSFETs . Since the
5 surface concentration of an implant region is highest as the surface 205', by
6 moving the P-deep region 405 higher in the structure, namely to abut the epitaxial
7 layer 205 surface 205', a lower breakdown voltage will be provided.

8 [0051] **FIGURE 5** is another embodiment of the present invention. The structure
9 500 depicts an arrangement of N-MOSFETs with integrated silicon controlled
10 rectifier ("SCR"). A pair 407, 409 of drain-connected N-channel MOSFETs (see
11 also FIGURE 2A, FIGURE 4) structure 500 is formed to include an N-well 501
12 segregating respective P-wells 209, 209' of the N-MOSFETs 407, 409; compare
13 also to FIGURE 1A.

14 [0052] In this embodiment, a P-deep region 525 is formed subjacent the drain
15 regions 213, 213' and within the N-well 501. Note that this forms a parasitic PNP
16 transistor using the P-deep region 525 as an emitter, the N-well 501 as a base,
17 and the P-well/epi/P-substrate layers 205/201 as a collector. P-deep region 525
18 dimensions can be tailored to achieve the desired SCR punch-through voltage
19 based on the specific implementation requirements, tuning the breakdown fields
20 and improving the PNP transistor gain accordingly.

21 [0053] NPN transistors are formed using each N+ source 211, 211' as an emitter,
22 each P-well 209, 209' as a base, and the drain N-well 501 as a collector. These
23 two bipolar transistors thus form an SCR between the drain and source of each

1 N-channel MOSFET. The addition of the P-deep region 525 in the N-well 501
2 has the effect of increasing the PNP transistor gain. Note also that the ESD
3 breakdown voltage, or in this case punch-through voltage of the SCR, can be
4 controlled by the spacing between the P-deep region 525 and P-wells 209, 209',
5 i.e., reduced by reducing the spacing and by depth of the P-deep region implant
6 into the N-well 501. In operation, during a positive ESD spike, +Ve, to the I/O pad
7 301, FIGURE 3, the SCR being in parallel with the N-channel MOSFETs can
8 conduct a significant amount of current, enhancing ESD protection.

9 [0054] FIGURES 6A and 6B illustrate the concept of the present invention in
10 BiCMOS technology exemplary embodiments. While a N-type epitaxial layer 605
11 is shown in both, it will be recognized by those skilled in the art that P-type
12 epitaxial layer implementations are known. These structures employ a buried
13 isolation layer, or region, 602 as is also known in the art. In FIGURE 6A, for N-
14 MOSFET construction, a parasitic lateral NPN transistors (see FIGURE 3, 315) -
15 from the N+ type doped drain region 613 forming the NPN collector, the MOSFET
16 body region, P-well 609, forming the NPN base, and the N+ type doped source
17 regions 611, 611' forming the grounded emitter - is provided with an increased
18 gain during breakdown by the addition of the P-deep region 625 subjacent the
19 drain region 613 in the P-well 609.

20 [0055] In FIGURE 6B, for P-MOSFET construction, a parasitic PNP transistor
21 (see FIGURE 3, 313) - from the P+ type doped drain region 613' forming the
22 emitter, the N-well/body 609' and N+ doped region 620 forming the base, and the
23 grounded P-substrate 201 forming the collector - is provided with increased gain

1 by the addition of the P-deep region 625' in the N-well 609' subjacent the P+
2 doped drain 613'. Note that the buried isolation layer 602 under the P-channel
3 MOSFET reduces the collector resistance and proximity to the P-deep region 625'
4 increases the gain of the PNP transistor.

5 [0056] FIGURE 7 is a representation of a BiCMOS technology structure 700 for a
6 push-pull I/O circuit with enhanced ESD protection. An N-MOSFET pair
7 incorporating a SCR (see also FIGURE 5) is again provided with a P-deep region
8 525 subposing the drain contact 215. Here note that an N-type doped buried
9 layer ("NBL") 701 pinches the P-well regions 209, 209'. This causes the P-well
10 resistance to be higher, resulting in a faster turn-on of the SCR. As with the
11 previous embodiments, particularly that of FIGURE 5, the added P-deep region
12 525 increases parasitic transistor gain accordingly, enhancing ESD protection
13 performance.

14 [0057] FIGURE 8 is a cross-sectional, elevation view, schematic of an extended
15 drain N-channel MOSFET structure in another exemplary embodiment of the
16 present invention. Extended and enhanced drain region devices, having reduced
17 on-resistance without significantly reducing breakdown voltage, are known, such
18 as from common assignees U.S. Pat. No. 5,517,046, filed by Hsing et al. for
19 HIGH VOLTAGE LATERAL DMOS DEVICE WITH ENHANCED DRIFT REGION,
20 incorporated herein by reference. As with prior embodiments herein, a P-deep
21 region 825 subjacent the N-well 809 containing the drain region 213. Note that it
22 should be recognized by those skilled in the art that the P-wells 209, 209' can be
23 P-body regions in a DMOS implementation such as in Hsing et al. As with the

1 embodiment described with respect to FIGURE 2A, there is a higher drain-to-
2 substrate inherent capacitance and enhanced parasitic NPN transistor gain in
3 breakdown of the structure compared to FIGURE 1A, providing a lower trigger
4 voltage for the N-MOSFETs, and enhancing ESD protection.

5 [0058] **FIGURE 9** is a cross-sectional, elevation view, schematic of a single N-
6 MOSFET structure in another exemplary embodiment in accordance with the
7 present invention. In some ICs, such as for power chips, it is known to have
8 relatively large arrays of single MOSFET structures 900 in an array configuration.
9 It is possible in accordance with the present invention to provide each individual
10 MOSFET structure 900 with a P-deep region 901 such as illustrated. In this
11 embodiment, the structure 900 is an example of a layout where the P-deep region
12 901 is implanted conveniently in association with the drain, D, region. It should
13 be expected that when using implant technology for forming the P-deep region
14 901 that the ion concentration will migrate toward the surface, shown as forming
15 a surface 205' concentration abutting the field oxide isolation 207' for the drain
16 region. Again, as with the embodiment described with respect to FIGURE 2A,
17 there is a higher drain-to-substrate inherent capacitance and enhanced parasitic
18 NPN transistor gain in breakdown of the structure compared to FIGURE 1A,
19 providing a lower trigger voltage for the N-MOSFETs, and enhancing ESD
20 protection.

21 [0059] The foregoing Detailed Description of exemplary and preferred
22 embodiments is presented for purposes of illustration and disclosure in
23 accordance with the requirements of the law. It is not intended to be exhaustive

1 nor to limit the invention to the precise form(s) described, but only to enable
2 others skilled in the art to understand how the invention may be suited for a
3 particular use or implementation. The possibility of modifications and variations
4 will be apparent to practitioners skilled in the art. Particularly, other MOS and
5 BiCMOS structures can be made by other arrangements wherein regional dopant
6 types are reversed to configure complementary structures. No limitation is
7 intended by the description of exemplary embodiments which may have included
8 tolerances, feature dimensions, specific operating conditions, engineering
9 specifications, or the like, and which may vary between implementations or with
10 changes to the state of the art, and no limitation should be implied therefrom.
11 Applicant has made this disclosure with respect to the current state of the art, but
12 also contemplates advancements during the term of the patent, and that
13 adaptations in the future may take into consideration those advancements, in
14 other word adaptations in accordance with the then current state of the art. It is
15 intended that the scope of the invention be defined by the Claims as written and
16 equivalents as applicable. Reference to a claim element in the singular is not
17 intended to mean "one and only one" unless explicitly so stated. Moreover, no
18 element, component, nor method or process step in this disclosure is intended to
19 be dedicated to the public regardless of whether the element, component, or step
20 is explicitly recited in the Claims. No claim element herein is to be construed
21 under the provisions of 35 U.S.C. Sec. 112, sixth paragraph, unless the element
22 is expressly recited using the phrase "means for. . ." and no method or process
23 step herein is to be construed under those provisions unless the step, or steps,

Docket No.: M081

- 1 are expressly recited using the phrase "comprising the step(s) of. . . ." What is
- 2 claimed is: